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OF

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FOR

DAMASCENE TRI-GATE FINFET

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TECHNICAL FIELD

[0001] The present invention relates generally to transistors and, more particularly, to fin field effect transistors (FinFETs).

BACKGROUND ART

[0002] The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

[0003] For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are, therefore, being explored to improve FET performance and allow further device scaling.

[0004] Double-gate MOSFETs represent structures that have been considered as candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, two gates may be used to control short channel effects. A FinFET is a recent double-gate structure that exhibits good short channel behavior. A FinFET includes a channel

formed in a vertical fin. The FinFET structure may be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

DISCLOSURE OF THE INVENTION

[0005] Implementations consistent with the present invention provide a tri-gate FinFET formed using, for example, a damascene process. A tri-gate FinFET will have better short-channel control than double-gate and single-gate devices, and will have higher drive current than a double-gate finFET for the same area. The metal tri-gate, formed in a damascene process consistent with the invention, may be used to reduce poly depletion effects and gate resistance.

[0006] Additional advantages and other features of the invention will be set forth in part in the description which follows and, in part, will become apparent to those having ordinary skill in the art upon examination of the following, or may be learned from the practice of the invention. The advantages and features of the invention may be realized and obtained as particularly pointed out in the appended claims.

[0007] According to the present invention, the foregoing and other advantages are achieved in part by a method of forming a fin field effect transistor that includes forming a fin and forming a source region adjacent a first end of the fin and a drain region adjacent a second end of the fin. The method further includes forming a dummy gate comprising a first material in a first pattern over the fin and forming a dielectric layer adjacent sides of the dummy gate. The method also includes removing the first material to form a trench in the dielectric layer corresponding to the first pattern and forming a metal gate in the trench.

[0008] According to another aspect of the invention, a tri-gate fin field effect transistor is provided. The tri-gate fin field effect transistor includes a fin that further

includes multiple surfaces and has a source region and a drain region formed adjacent each end of the fin. The tri-gate fin field effect transistor further includes a metal gate formed on three surfaces of the multiple surfaces.

[0009] According to an additional aspect of the invention, a method of forming a fin field effect transistor includes forming a fin and forming a source region adjacent a first end of the fin and a drain region adjacent a second end of the fin. The method further includes forming a dummy oxide layer over the fin, depositing a layer of first material over the fin and dummy oxide layer, and etching the layer of the first material to form a dummy gate in a first pattern. The method also includes depositing a dielectric layer over the dummy gate and source and drain regions, planarizing the dielectric layer to expose a top surface of the dummy gate, and removing the first material to form a trench in the dielectric layer corresponding to the first pattern. The method additionally includes forming a gate insulation layer in the trench and forming a metal gate in the trench.

[0010] Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

[0012] FIG. 1 illustrates exemplary layers of a silicon-on-insulator (SOI) wafer that may be used for forming a fin of a FinFET consistent with the present invention;

[0013] FIG. 2A illustrates an exemplary fin consistent with the invention;

[0014] FIGS. 2B and 2C illustrate source and drain regions formed adjacent the fin of FIG. 2A consistent with the invention;

[0015] FIG. 2D illustrates a cross-sectional view of the exemplary fin of FIG. 2A consistent with the invention;

[0016] FIG. 3A illustrates a cross-sectional view of a layer of sacrificial oxide formed on the fin of FIG. 2A consistent with the invention;

[0017] FIG. 3B illustrates a cross-sectional view of the removal of the sacrificial oxide of FIG. 3A consistent with the invention;

[0018] FIGS. 4A and 4B illustrate cross-sectional views of dummy oxide and a polysilicon layer formed on the fin of FIG. 3B consistent with the invention;

[0019] FIGS. 5A and 5B illustrate the formation of a dummy gate from the polysilicon layer of FIG. 4B consistent with the invention;

[0020] FIG. 6 illustrates the formation of a dielectric layer adjacent the dummy gate of FIGS. 5A and 5B consistent with the present invention; and

[0021] FIG. 7 illustrates the removal of the dummy gate of FIGS. 5A and 5B to form a gate trench consistent with the present invention;

[0022] FIG. 8 illustrates formation of gate insulation within the gate trench of FIG. 7 consistent with the present invention;

[0023] FIGS. 9A, 9B and 9C illustrate formation of a metal tri-gate within the gate trench of FIG. 8 consistent with the present invention;

[0024] FIG. 10 illustrates formation of a polysilicon layer over a fin consistent with another embodiment of the invention;

[0025] FIG. 11 illustrates planarization of the polysilicon layer of FIG. 10 consistent with another embodiment of the invention;

[0026] FIG. 12 illustrates removal of the cap of FIG. 11 consistent with another embodiment of the invention; and

[0027] FIG. 13 illustrates formation of a layer of polysilicon, with controlled thickness, over the fin and planarized polysilicon layer of FIG. 12 consistent with another embodiment of the invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0028] The following detailed description of the invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims.

[0029] Consistent with the present invention, an exemplary damascene process for forming a tri-gate FinFET is provided. In the exemplary damascene process, a dummy gate may be formed from a layer of semi-conducting material, such as, for example, polysilicon, that has been formed over a fin. A dielectric layer may then be formed over the FinFET fin, source and drain regions around the dummy gate. The dummy gate may then be removed to create a gate trench in the dielectric layer. A metal gate that contacts three surfaces of the fin may then be formed in the created gate trench to complete the damascene process.

[0030] FIG. 1 illustrates a cross-section of a silicon on insulator (SOI) wafer 100 formed in accordance with an exemplary embodiment of the present invention. SOI wafer 100, consistent with the present invention, may include a buried oxide layer 110

formed on a substrate 115. A fin layer 105 may further be formed on buried oxide layer 110. The thickness of fin layer 105 may range, for example, from about 500Å to about 2000Å and the thickness of buried oxide layer 110 may range, for example, from about 1000Å to about 3000Å. Fin layer 105 and substrate 115 may include, for example, silicon, though other semi-conducting materials, such as germanium, may be used.

[0031] As shown in FIGS. 2A and 2D, a vertical fin 205 may be formed from fin layer 105. Fin 205 may be formed, for example, with a width (w) in a range of 10-50 nm. Fin 205 may be formed from fin layer 105 using any conventional process, including, but not limited to, conventional photolithographic and etching processes.

[0032] Subsequent to formation of fin 205, source 210 and drain 215 regions may be formed adjacent respective ends of fin 205, as shown in FIGS. 2B and 2C. Source 210 and drain 215 regions may be formed by, for example, deposition of a layer of semi-conducting material over fin 205. The source 210 and drain 215 regions may be formed from the layer of semi-conducting material using, for example, conventional photolithographic and etching processes. One skilled in the art will recognize, however, that other existing techniques may be used for forming source 210 and drain 215 regions. For example, source 210 and drain 215 regions may be formed by patterning and etching fin layer 105. Source 210 and drain 215 regions may include a semi-conducting material such as, for example, silicon, germanium or silicon-germanium (Si-Ge). In one implementation, $Si_xGe_{(1-x)}$, with x approximately equal to 0.7 may be used. A cap 220 may then be formed on upper surfaces of fin 205, source 210 and drain 215, as illustrated in FIG. 2D. Cap 220 may include an oxide, such as, for example, silicon oxide, and may range, for example, from about 150 Å to about 700 Å in thickness.

[0033] After formation of source 210 and drain 215 regions, a sacrificial oxide layer 305 may be formed on fin 205, source 210 and drain 215, as shown in FIG. 3A. Sacrificial oxide layer 305 may be formed on fin 205, source 210 and drain 215 using any appropriate conventional process. In some exemplary embodiments, for example, oxide layer 305 may be thermally grown on fin 205, source 210 and drain 215 to a thickness ranging from about 50 Å to about 150 Å. As shown in FIG. 3B, cap 210 and sacrificial oxide layer 305 may be removed using a conventional process, such as, for example, a conventional etching process to remove defects from sidewalls of fin 205.

[0034] Dummy oxide 405 may be formed on fin 205, source 210 and drain 215 using a conventional process, as shown in FIG. 4A. Dummy oxide 405, for example, may be thermally grown on fin 205, source 210 and drain 215. Dummy oxide 405 may include an oxide, such as, for example, silicon oxide and may range, for example, from about 50 Å to about 150 Å in thickness. As further shown in FIG. 4B, a layer of polysilicon 410 may be formed over fin 205, source 210 and drain 215. The thickness of polysilicon layer 410 may range, for example, from about 700 Å to about 2000 Å. Polysilicon layer 410 may be polished back using, for example, a chemical-mechanical polishing (CM) process, to achieve a planar surface to improve subsequent gate lithography. As shown in FIGS. 5A and 5B, a dummy gate 505 may be defined in polysilicon layer 410 using a conventional process, such as, for example, a conventional patterning and etching process.

[0035] As shown in FIG. 6, a dielectric layer 605 may be formed over dummy gate 505 using, for example, conventional deposition processes. Dielectric layer 605 may include, for example, tetraethylorthosilicate (TEOS), or any other dielectric material. The thickness of dielectric layer 605 may range, for example, from about

1000 Å to about 2500 Å. Dielectric layer 605 may then be polished back to the upper surface of dummy gate 505 using, for example, a CMP process, as illustrated in FIG. 6.

[0036] Dummy gate 505 and dummy oxide 405 may then be removed, as shown in FIG. 7, leaving a gate trench 705. Dummy gate 505 and dummy oxide 405 may be removed using, for example, conventional etching processes. Gate insulation 710 may then be formed in gate trench 705, as shown in FIG. 8. Gate insulation 710 may be thermally grown or deposited using conventional deposition processes. Gate insulation 710 may include SiO, SiO_2, SiN, SiON, HFO_2, ZrO_2, Al_2O_3, HFSiO(x) ZnS, MgF_2, or other high-K dielectric materials.

[0037] As shown in FIGS. 9A, 9B and 9C, a metal gate 905 may be formed in gate trench 705 over gate insulation 710. Metal gate 905 may be formed in gate trench 705 using a conventional metal deposition process and polished back to the upper surface of dielectric layer 605. Metal gate 905 may include a metal material, such as, for example, TaN or TiN, though other metal materials may be used. As shown in FIG. 9C, the resulting metal gate 905 is disposed on all three sides of fin 205, thus, producing a tri-gate FinFET. The tri-gate FinFET, consistent with the invention, will have better short-channel control than double-gate and single-gate devices. The tri-gate FinFET also has higher drive current than a double-gate FinFET for the same area. The metal gate 905 of the tri-gate FinFET also reduces poly depletion effects and gate resistance.

EXEMPLARY SELF-STOPPING POLY PLANARIZATION

[0038] FIGS. 10-13 illustrate an exemplary self stopping poly planarization process for forming a FinFET, consistent with another embodiment of the present invention, that leaves the FinFET gates connected after planarization. As shown in

FIG. 10, the exemplary process may begin with the deposition of a thin layer of oxide or nitride on a fin 1005. Fin 1005 may be formed in accordance with the exemplary process described above with respect to FIGS. 1 and 2. The thin layer may include an oxide or nitride material and may range, for example, from about 150 Å to about 700 Å in thickness. Subsequent to deposition of the thin layer of oxide or nitride, the layer may be patterned and etched, using conventional processes, to produce a cap 1010 on fin 1005. A layer of polysilicon 1015 may then be formed over cap 1010 and fin 1005 using, for example, conventional deposition processes. As shown in FIG. 11, the layer of polysilicon 1015 may be planarized back to an upper surface of cap 1010 using, for example, a highly selective poly to oxide CMP process. Cap 1010 may function as a polish stop layer. Polysilicon layer 1015 may function as the gate material.

[0039] Cap 1010 may then be stripped using, for example, a conventional etching process, as shown in FIG. 12. A uniformly thin layer of polysilicon 1305 may then be formed over fin 1005 and planarized polysilicon layer 1015, as shown in FIG. 13, using conventional deposition processes. Using the above exemplary process, the thickness of the polysilicon 1305 over fin 1005 may be carefully controlled. Polysilicon 1305 may connect the gates located on either said of fin 1005.

[0040] In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional photolithographic, etching and deposition techniques

may be employed, and hence, the details of such techniques have not been set forth herein in detail.

[0041] Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.